

TSMC-00-284B



September 24, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/613,607 07/03/03

Kuo-Reay Peng, Jian-Hsing Lee

DEPLETION MODE SCR FOR LOW
CAPACITANCE ESD INPUT PROTECTION

Grp. Art Unit: -----

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

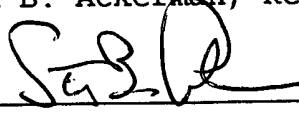
The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on September 26, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 9/26/03

The following four U.S. Patents pertain to ESD protection:

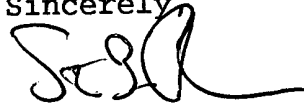
- 1) U.S. Patent 5,537,284 to Haas, Jr. et al.,
"Electrostatic Discharge Protection Device."
- 2) U.S. Patent 5,821,572 to Walker et al., "Simple BICMOS
Process for Creation of Low Trigger Voltage SCR and
Zener Diode Pad Protection."
- 3) U.S. Patent 5,825,600 to Watt, "Fast Turn-On Silicon
Controlled Rectifier (SCR) for Electrostatic Discharge
(ESD) Protection."
- 4) U.S. Patent 6,074,899 to Voldman, "3-D CMOS-on-SOI ESD
Structure and Method."

The following three technical reports refer to the subject
of ESD protection in MOS circuits:

- 1) Wu et al., "ESD Protection for Output Pad with Well-
Coupled Field-Oxide Device in 0.5- μm CMOS
Technology," IEEE Transactions on Electron Devices,
Vol. 44, No. 3, pp. 503-508, March 1997, IEEE.

- 2) Ker et al., "ESD Protection Design on Analog Pin with Very Low Input Capacitance for High-Frequency or Current-Mode Applications," IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, pp. 1194-1199, August 2000, IEEE.
- 3) Kleveland et al., "Distributed ESD Protection for High-Speed Integrated Circuits," IEEE Electron Device Letters, Vol. 21, No. 8, pp. 390-392, August 2000, IEEE.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', with a long horizontal flourish extending to the right.

Stephen B. Ackerman,
Reg. No. 37761

SEP 29 2008
OIPF
PATENT & TRADEMARK OFFICE

Duchas (Humboldt) (Cyprianus)

Application Number

10/613, 607

Applicant:

Applicant: Kuo-Reay Peng et al.

FD-302 (Rev. 11-27-70)

07/03/03

Group 11 Unit

EXAMINER
IN THE TRADE

EXAMINER
IN THE TRADE

Year	United States	Japan	Germany
1950	7	15	18
1960	8	16	19
1970	9	17	20
1980	10	18	21
1990	11	19	21
2000	12	19	21
2010	13	19	21
2020	14	19	21
2030	14	19	21
2040	15	20	22
2050	15	20	22

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1950	7	15	18
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1990	11	19	21
2000	12	19	21
2010	13	19	21
2020	14	19	21
2030	14	19	21
2040	15	20	22
2050	15	20	22

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2000, IEEE -

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant

SEP 29 1963

Hydrogen Number

10/613, 607

Kuo-Beau Peng et al.

07/03/03

Ordering Unit

several shows if necessary)

~~SECRET~~

DOCUMENT NUMBER

DATE

COUNTRY

CLASS

SUBCLASS

Translation

YES

42

(Including Author, Title, Date, Portion or Pages, Etc.)

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Kleveland et al., "Distributed ESD Protection for High-Speed Integrated Circuits," IEEE Electron Device Letters, Vol. 21, No. 8, Aug. 2000, IEEE.

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.